



# UNITED STATES PATENT AND TRADEMARK OFFICE

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UNITED STATES PATENT AND TRADEMARK OFFICE  
WASHINGTON, D.C. 20231  
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\*BIBDATASHEET\*

CONFIRMATION NO. 1388

Bib Data Sheet

SERIAL NUMBER 09/855,660	FILING DATE 05/16/2001  RULE	CLASS 326	GROUP ART UNIT 2819	ATTORNEY DOCKET NO. XA-9472
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## APPLICANTS

Yasuhisa Shimazaki, Tokyo, JAPAN;

Motoi Ichihashi, Tachikawa, JAPAN;

\*\* CONTINUING DATA \*\*\*\*\*

*OC Nme*

\*\* FOREIGN APPLICATIONS \*\*\*\*\*

JAPAN 2000-152732 05/19/2000

*OC*

IF REQUIRED, FOREIGN FILING LICENSE GRANTED

\*\* 07/12/2001

Foreign Priority claimed

☒ yes ☐ no

35 USC 119 (a-d) conditions met

☒ yes ☐ no

☐ Met after Allowance

Verified and Acknowledged

Examiner's Signature

*OC*

STATE OR

COUNTRY  
JAPAN

SHEETS

DRAWING  
22

TOTAL

CLAIMS  
42

INDEPENDENT

CLAIMS  
11

## ADDRESS

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## TITLE

SEMICONDUCTOR INTEGRATED CIRCUIT HAVING HIGH-SPEED AND LOW-POWER LOGIC GATES WITH COMMON TRANSISTOR SUBSTRATE POTENTIALS, AND DESIGN DATA RECORDING MEDIUM THEREFOR

FILING FEE

RECEIVED  
2286

FEES: Authority has been given in Paper  
No. \_\_\_\_\_ to charge/credit DEPOSIT ACCOUNT  
No. \_\_\_\_\_ for following:

☐ All Fees

☐ 1.16 Fees ( Filing )

☐ 1.17 Fees ( Processing Ext. of time )

☐ 1.18 Fees ( Issue )

☐ Other \_\_\_\_\_